

Fig 1. Semiconductor device
(in the independent claim 39 etc.)

SKETCH A

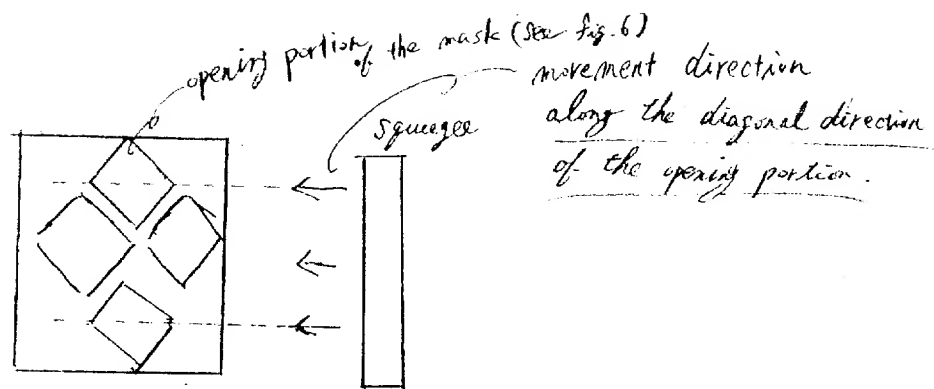


Fig. forming of insulating layer by mask-printing (in the claims ^{50 and 62})
(see the figs. 6. and 7)

SKETCH B

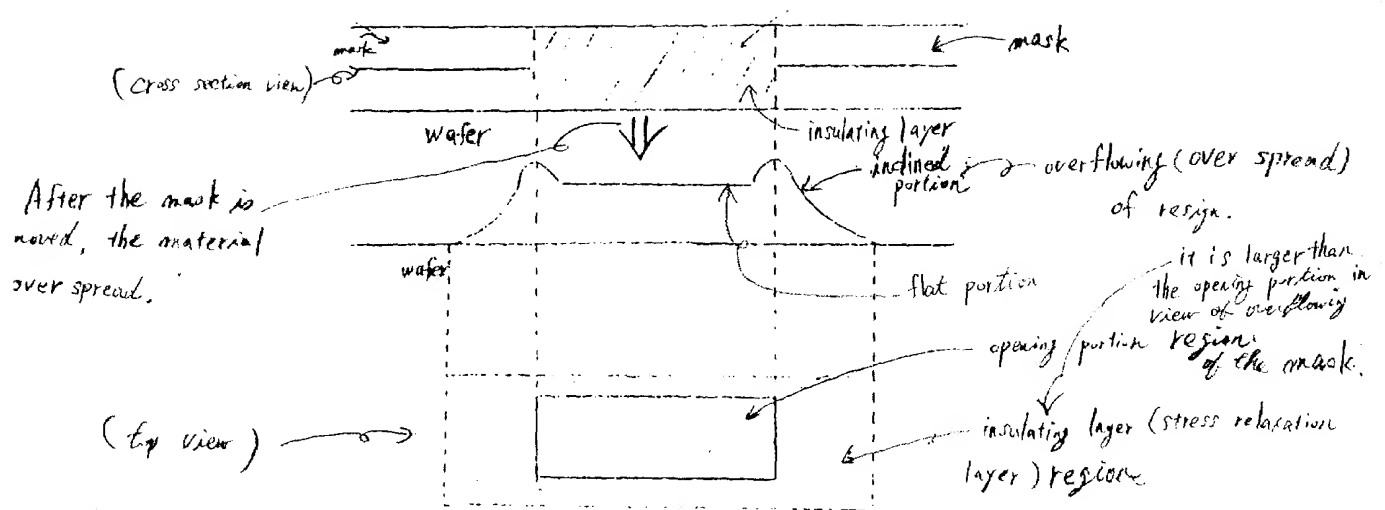


Fig. forming of a stress relaxation layer (in the claim 52 and 64)

SKETCH C

FIG. 4

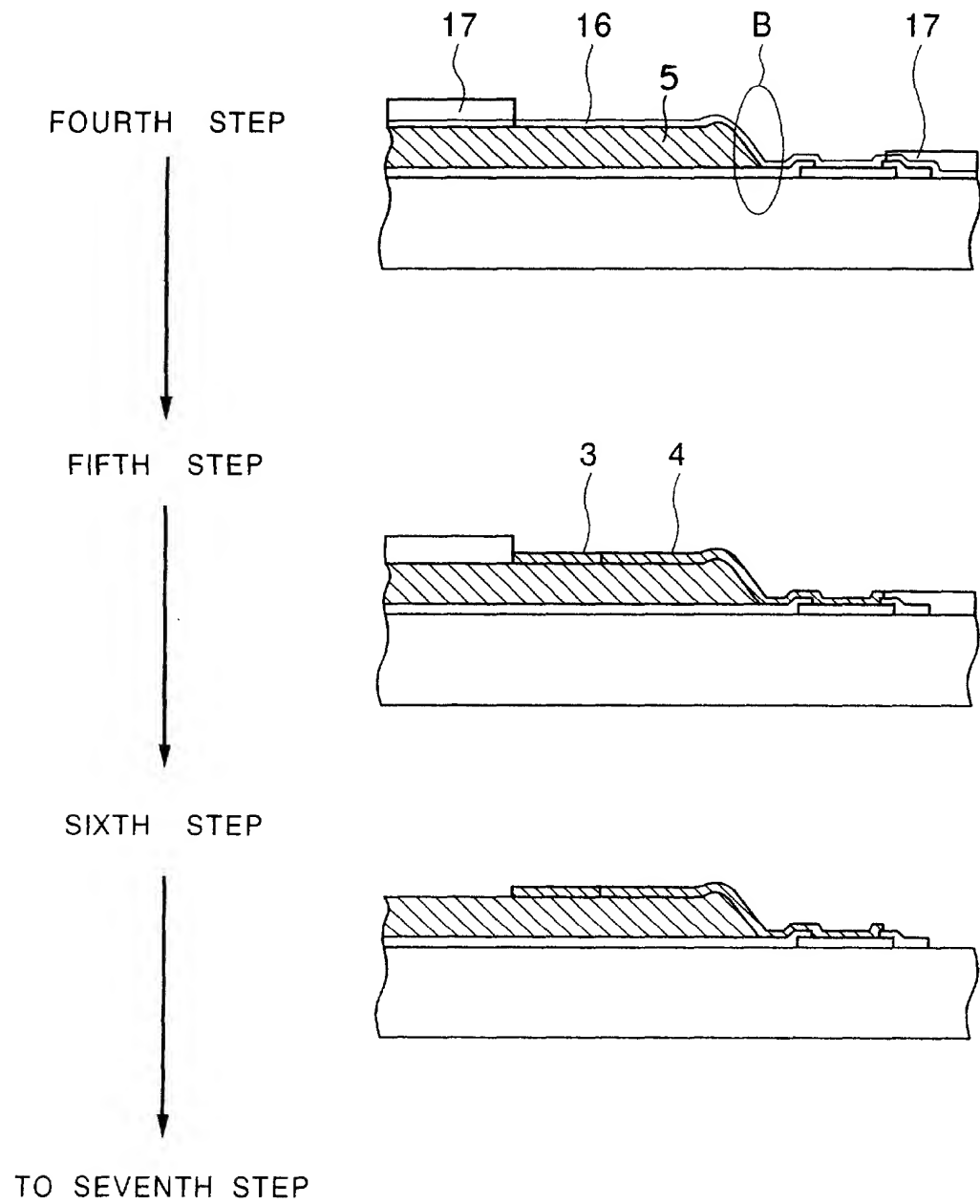


FIG. 31
(PRIOR ART)

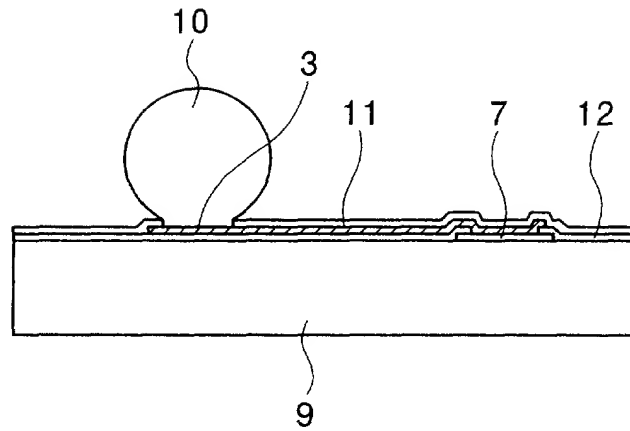


FIG. 32
(PRIOR ART)

